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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/338,286	06/22/1999	RICHARD SNOW	IGT1P073/P-229	1185

79646 7590 04/27/2009

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EXAMINER	
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ART UNIT	PAPER NUMBER
3714	

MAIL DATE	DELIVERY MODE
04/27/2009	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte RICHARD SNOW and STEVEN SHAFFER

Appeal 2008-3056
Application 09/338,286
Technology Center 3700

Decided:[1] April 27, 2009

Before DONALD E. ADAMS, LORA M. GREEN, and JEFFREY N. FREDMAN, *Administrative Patent Judges*.

Opinion for the Board filed by GREEN, *Administrative Patent Judge.*

Opinion Dissenting filed by FREDMAN, *Administrative Patent Judge.*

GREEN, *Administrative Patent Judge.*

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 10, 11, 15, 16, and 20-24. We have jurisdiction under 35 U.S.C. § 6(b).

STATEMENT OF THE CASE

The claims are directed to a gaming machine. Claim 10 is representative of the claims on appeal, and read as follows:

10. A gaming machine comprising:
a housing;
a user input connected to the housing;
a display connected to the housing; and
a control system located within the housing, the control system comprising a processing platform that comprises:
a mother board, said motherboard comprising;
a first processor;
a memory wherein the first processor and the memory are designed or configured to control and operate one or more of i) visual displays, ii) attraction animation features, iii) audio player feedback, iv) real-time video presentations, v) and operating system and combinations thereof;
one or more buses on the more on the motherboard wherein each of the one or more buses uses an interface protocol selected from a group consisting of peripheral component interconnect (PCI), industrial standard architecture (ISA), Versa Module Europa (VME), and accelerated graphics port (AGP);
one or more expansion slots for connecting a board to the buses;
a gaming processing subsystem designed to control a game played on the gaming machine, the gaming processing subsystem comprising,
a first gaming processing subsystem board connected to one of the buses on the motherboard, the first gaming processing subsystem board comprising;

a second processor designed or configured to control the gaming machine and to control Input/Output to the gaming machine;

a non-volatile memory for storing at least payout information;

a data memory socket located on the first gaming processing subsystem board designed to accommodate a data prom; and

a bus interface for connecting the first gaming processing subsystem board to one of the buses via one of the expansion slots on the motherboard

wherein the first gaming processing subsystem board is designed to control one or more of: i) a game play history, ii) gaming machine access, iii) user interface devices, iv) money handling devices, v) gaming machine I/O communications, v) random number generation and vi) progressive jackpot information.

The Examiner relies on the following evidence:

Byers	US 5,788,509	Aug. 4, 1998
Weiss	US 6,071,190	Jun. 6, 2000

Newton's Telecom Dictionary 751 (14th ed. 1998).

We reverse.

ISSUE(S)

The Examiner concludes that claims 10, 11, 15, 16, 20, 21, and 24 are rendered obvious by the combination of Weiss and Byers; and that claims 22 and 23 are rendered obvious by the combination of Weiss and Byers, as further combined with Newton's Telecom Dictionary.

Appellants contend that the references, either alone or in combination, establish that it would have been obvious to the ordinary artisan to replace the encrypted serial and/or parallel interface with a bus interface.

Thus, the issue on Appeal is: Has the Examiner established a prima facie case that the references, either alone or in combination, establish that it would have been obvious to the ordinary artisan to replace the encrypted serial and/or parallel interface with a bus interface?

FINDINGS OF FACT

FF1 According to the Specification:

> A processing platform for operation of a gaming machine in accordance with the present invention includes a bus, a gaming processing subsystem for controlling aspects of gaming machine operation that involve game functionality and thus are generally subject to regulation coupled to the bus and a general computing subsystem for controlling aspects of gaming machine operation that do not involve game functionality and thus are not generally subject to regulation. The general computing subsystem is also coupled to the bus and the gaming processing subsystem is physically separate from the general computing subsystem.

(Spec. 2.)

FF2 The Examiner rejects claims 10, 11, 15, 16, 20, 21, and 24 under 35 U.S.C. § 103(a) as being rendered obvious by the combination of Weiss and Byers (Ans. 3).

FF3 The Examiner finds that "Weiss discloses all of the instant application without specifically disclosing how the various processing subsystems are connected such as the use of a motherboard with expansion slots and a serial UART." (*Id.*)

FF4 According to the Examiner, Weiss teaches that "a need exists for an open architecture design, for example, a personal computer based design . . .

of the gaming device which would provide all shell functions of presenting the game environment and thus providing a substantial entertainment component of the gaming device." (*Id.* at 3-4.)

FF5 Specifically, as to claim 10, the Examiner finds that Weiss discloses "a housing 100, a plurality of user inputs, a display 50, a gaming processing subsystem is a secure processing area 60 which includes a processor board 162 and a main board 164 which controls the display and sound generated connected by a bus to a back plane 166." (*Id.* (citing Weiss, Figs. 2 and 6, cols. 6, 11, and 12).)

FF6 The Examiner also finds that "Weiss teaches that it is obvious to use a plurality of processing platforms constructed to be in communication with each other to provide security and be expandable for other gaming functions," and that it "would have been obvious to one of ordinary skill in the art . . . to use the teachings of Weiss to connect the various processing systems such as by using a personal computer based design." (Ans. 4.)

FF7 Weiss is drawn to a gaming device, and in particular:

> [T]o an advanced video and slot gaming device security system having dual processing areas with a master/slave relationship wherein the master includes a secure processing area including critical gaming functions stored and executed from a non-alterable media by the secure processing area while allowing the slave processing area to have an open architecture which is expandable without compromising critical gaming functions and retaining the ability for regulatory validation of the secure processing area of the system.

(Weiss, col. 1, ll. 6-15.)

FF8 Weiss teaches:

> Today's trend in gaming devices is towards an increasing utilization of personal computer based gaming platforms. Personal computer based platforms are being employed by designers to make use of real time operating systems which allow for multi-threaded/multi-tasking processes and the use of many "off the shelf" device drivers. While at first, this may seem an advantage, it is not a wise choice in an environment requiring high security and regulatory monitoring. Designs of this nature elude validation by regulatory authorities in two areas, initial laboratory evaluation and field validation. Any in depth review of a PC based gaming device is both difficult and far from definitive, requiring tremendous engineering resources and specialist in computer security which are expensive and normally available only on a consultant basis. Even if these resources were available, it is impossible to study the hundreds of thousands of lines of source code comprising all of the elements of such a system. In addition, the time involved in just learning how to build the executable code from the source for correlation is time and resource prohibited. The multi-threaded/multi-tasking process nature of the programs in these devices make it extremely difficult to locate any compromising code which becomes clandestine since the actual sequence of the execution is hidden to the evaluating engineer. Furthermore, the code set for a complex PC device may not be fully embraced by the evaluating engineer.

(*Id.* at col. 1, l. 46-col. 2, l. 4.)

FF9 Thus, according to Weiss:

> [A] need exists for an independent secured processor design for validation which would provide all key functions such as the determination of game outcome, monetary input, output, and logging of relevant events. Furthermore, a need exists for an open architecture design, for example, a personal computer based design of the gaming device which would provide all shell functions of presenting the game environment and thus providing a substantial entertainment component of the gaming device. Therefore, even though compromise is still possible at

> the shell level, evidence of what should have occurred is recoverable from the specially designed secured processor.

(*Id.* at col. 2, ll. 46-57.)

FF10 Weiss teaches the use of two processing areas that are linked together through a secure protocol (*id.* at col. 2, ll. 60-64). One of the processing areas includes non-alterable storage media having gaming critical functions, and the other processing area includes an open architecture design that may be expanded without comprising the critical gaming functions (*id.* at col. 2, l. 64-col. 3, l. 3).

FF11 Weiss refers to the first processing area as a white box, and the second, secure processing area as a black box (*id.* at col. 7, l. 66-col. 8, l. 1).

FF12 Figure 6 of Weiss, showing the second processing area, is reproduced below:

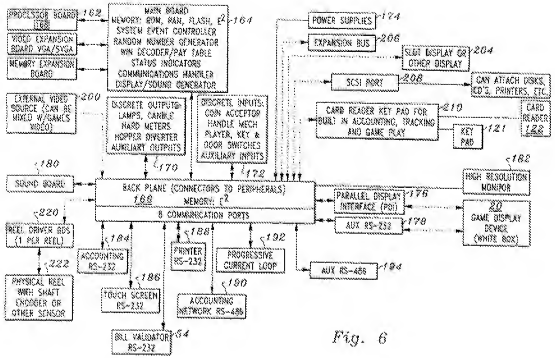

Fig. 6

Figure 6 is a detailed block diagram of the second processing system according to one aspect of the invention (*id.* at col. 5, ll. 64-65).

FF13 The secure processing area includes "a processor board **162**, a main board **164** and a back plane **166** integrally or separately formed." (*Id.* at col. 11, ll. 33-35.)

FF14 The "processor board **162** includes a graphics system processor **168** which is operatively coupled to the main board **164**." (*Id.* at col. 11, ll. 36-38.)

FF15 The main board **164** "includes memory in the form of ROM. RAM, flash memory and EEPROM," as well as "a system event controller, the random number generator **62**, a win decoder/pay table, status indicators, a

communications handler and a display/sound generator." (*Id.* at col. 11, ll. 38-45.)

FF16 The main board **164** is connected to the back plane **166**, and the back plane provides a plurality of communication ports for communicating with external peripherals (*id.* at col. 11, ll. 46-60).

FF17 Figure 7 of Weiss is reproduced below:

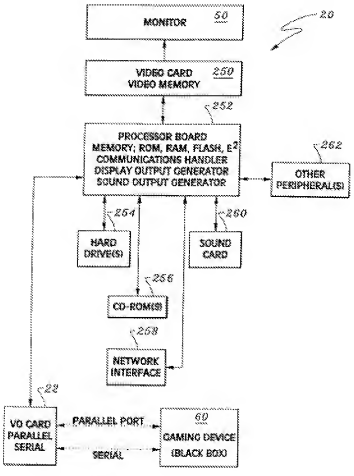

Fig. 7

Figure 7 is a detailed block diagram of the first processing system according to one aspect of the invention (*id.* at col. 5, ll. 66-67).

FF18 The first processing system (white box) may be "an interactive multi-media gaming computer which includes the first processing area **20**," which "includes an input/output parallel and serial card **22**." (*Id.* at col. 12, ll. 15-18.)

FF19 The processing system also has a processor board **252**, which "includes memory in the form of read only memory, the dynamic random access memory **26** and internal alterable program storage media **24**," as well as "a communications handler, a display output generator and a sound output generator." (*Id.* at col. 12, ll. 15-29.)

FF20 Weiss teaches that the "processor board also allows peripherals in the form of, for example, hard drives **254**, CD ROMS **256**, network interfaces **258**, sound cards **260** and other desirable peripherals **262** for game enhancement and patron entertainment." (*Id.* at col. 12, ll. 31-34.)

FF21 The first and second processing systems are connected by a communication link that is for transmitting encrypted data (*id.* at col. 6, ll. 16-22), thus precluding any alteration of critical gaming functions (*id.* at col. 7, ll. 7-11).

FF22 Weiss teaches that communication between the black and white box is via a parallel display interface and/or a serial interface (*id.* at col. 11, ll. 65-67).

FF23 The Examiner finds that the secure processing system shows a main board, that can be equated to a motherboard, but finds that the first processing system of Weiss (the white box as shown in Figure 7) "comprises a processor board (252) with no mention of the processing board being a 'motherboard' or a 'main board.'" (Ans. 7.)

FF24 The Examiner finds further that as the white box and black box of Weiss have a master/slave configuration in one regard, as the second processing area (the black box) initiates all messages, while the second processing area is the slave (*id.*).

FF25 Thus, the Examiner appears to be reading the second processing system as shown in Figure 6 of Weiss as the mother board of claim 10, and the first processing system as shown in Figure 7 as the gaming processing subsystem as the gaming processing subsystem of claim 10.

FF26 The Examiner cites Byers, which the Examiner finds is an analogous invention, for teaching that "it is known to attach to a motherboard Industry Standard Architecture (ISA) expansion cards that connect the computer electronics to the peripheral device." (Ans. 5.)

FF27 Specifically, Byers teaches "an apparatus that provides audio connectors to a motherboard of a computer." (Byers, col. 1, ll. 11-13.)

FF28 The Examiner concludes that it "would [have been] obvious to one of ordinary skill in the art at the time of the invention to have a pc computer with a motherboard capable of accepting cards using the motivation provided by Weiss that a computer backplane could be integrally or separately formed on the main board (motherboard) and that other desired peripherals for game enhancement and patron entertainment could be added to the main board." (Ans. 5.)

FF29 The Examiner also rejects claims 22 and 23 under 35 U.S.C. § 103(a) as being obvious over the combination of Weiss and Byers, as further combined with Newton's Telecom Dictionary (*id.*).

FF30 The Examiner relies on Newton's Telecom Dictionary for the definition of UART.

PRINCIPLES OF LAW

The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) secondary considerations of nonobviousness, if any. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966).

While the analysis under 35 U.S.C. § 103 allows flexibility in determining whether a claimed invention would have been obvious, *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007), it still requires showing that "there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *Id.* "We must still be careful not to allow hindsight reconstruction of references to reach the claimed invention without any explanation as to how or why the references would be combined to produce the claimed invention." *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 n.3 (Fed. Cir. 2008).

ANALYSIS

Appellants argue further that contrary to the Examiner's finding that Weiss does not disclose how the various processing subsystems are connected (*see, e.g.*, FF3), "Weiss specifies that the communication link . . . between the first processing area and the second processing area, is via the

parallel display interface 176 and/or the RS-232 serial interface." (App. Br. 7.)

According to Appellants, Weiss explains why a PC based design is not desirable, due to a high security environment and regulatory monitoring (*Id.* at 12 (quoting Weiss, col. 1, l. 46-col. 2, l. 35); *see also* FF 8). Appellants argue further that Weiss notes that "it is impossible to study the hundreds of thousands of lines of source code comprising the elements of [a PC based gaming system," thus making PC based devices not field verifiable (App. Br. 13 (quoting Weiss col. 1, l. 46-col. 2, l. 4.); *see also* FF8).

We find that Appellants have the better position, and conclude that the Examiner has not set forth a prima facie case that Weiss teaches or suggests that it would have been obvious to the ordinary artisan to replace the encrypted serial and/or parallel interface of Weiss with a bus interface. We acknowledge that, as evidenced by Byers (*see* FF26), the use of bus interfaces are known in the art. But the Examiner has not provided evidence or scientific reasoning that it would have been obvious to the ordinary artisan to replace the serial and/or parallel interface of Weiss, which is encrypted and precludes the alteration of critical gaming functions (FF21), and used to connect the processing area that includes non-alterable storage media having gaming critical functions with the more open processing area that includes an open architecture design that may be expanded without comprising the critical gaming functions (*see* FF9, FF10), with a bus that uses an interface protocol selected from PCI, ISA, IME, or AGP, as required by claim 10.

Moreover, Newton's Telecom Dictionary, which was cited for its definition of UART (FF27, FF28), does not remedy the deficiencies of the combination of Weiss and Byers as set forth by the Examiner.

CONCLUSION(S) OF LAW

We conclude that the Examiner has not established a prima facie case that the references, either alone or in combination, establish that it would have been obvious to the ordinary artisan to replace the encrypted serial and/or parallel interface as taught by Weiss with a bus interface as taught by Byers.

We are thus compelled to reverse the rejection of claims 10, 11, 15, 16, 20, 21, and 24 under 35 U.S.C. § 103(a) as being rendered obvious by the combination of Weiss and Byers; as well as the rejection of claims 22 and 23 under 35 U.S.C. § 103(a) as being obvious over the combination of Weiss and Byers, as further combined with Newton's Telecom Dictionary.

REVERSED

cdc

DISSENTING OPINION

Fredman,

Administrative Patent Judge

I respectfully dissent from the Majority's obviousness analysis in the instant situation and would affirm the Examiner's rejection under 35 U.S.C. § 103(a).

The Majority finds that the "Examiner has not set forth a prima facie case that Weiss teaches or suggests that it would have been obvious to the ordinary artisan to replace the encrypted serial and/or parallel interface of Weiss with a bus interface." (Majority Opinion Supra.) The Majority supports this conclusion based on the fact that "the Examiner has not provided evidence or scientific reasoning that it would have been obvious to the ordinary artisan to replace the serial and/or parallel interface of Weiss, which is encrypted and precludes the alteration of critical gaming functions" (Majority Opinion Supra).

ADDITIONAL PRINCIPLES OF LAW

"The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR*, 550 U.S. at 416. "If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability." *Id.* at 417. Moreover, an "[e]xpress suggestion to substitute one equivalent for another need not be present to render such substitution obvious." *In re Fout*, 675 F.2d 297, 301 (CCPA 1982). As noted by the Court in *KSR*, "[a] person of

ordinary skill is also a person of ordinary creativity, not an automaton." 550 U.S. at 421.

ADDITIONAL FINDING OF FACT

FF31 The Examiner finds that the "use of PCI, ISA, VME, or AGP in order to connect peripherals to a bus are well known standards in the computing arts and will be treated as analogous interface protocols" (Ans. 4).

DISCUSSION

In my opinion, Weiss teaches all of the elements of the claim except for the use of a PCI bus (FF6-25) and Byers teaches using a bus to connect two boards with different functions (FF26-27). Consistent with *KSR*, all of the elements of this invention are known and the use of alternative connections between two different boards is known (FF31). Consequently, the person of ordinary skill in this art, a computer programmer or hardware designer, who is a person of no more than ordinary creativity, would have recognized that a PCI bus could predictably have been substituted for an RS-232 interface.

When Appellants argue regarding the RS-232 interface that "these types of interfaces are slow and are not designed to handle large amounts of information, i.e., this type of connection is very different from the connection provided by an expansion slot on a motherboard as recited in the present invention" (App. Br. 7), I contend that this argument supports the rejection. The person of ordinary skill and ordinary creativity at the time of invention would have been motivated to substitute well known and faster interfaces such as PCI, ISA, VME or AGP for the slower RS-232 interface.

I am also not convinced by Appellants' argument regarding the differences between the Weiss invention and the claims, since the claims simply require the different PCI, ISA, VME or AGP interface between the motherboard and the "gaming subsystem" (Claim 10). As discussed in the findings of fact in the Majority Opinion, Weiss teaches a motherboard and a distinct "gaming subsystem" as represented by the "black" and "white" boxes (FF11-18).

I also do not find persuasive Appellants' argument that "[t]o allow the secure processing of Weiss to be plugged into an expansion slot on the motherboard of its open processing area . . . the secure processing area would have to be totally redesigned" (App. Br. 8). In any computer or slot machine, the expansion slots, whether for a "gaming subsystem" or a sound card, must be designed to receive the appropriate size sub-boards. The ordinary artisan would have been reasonably able to design expansion slots to accept whatever size "gaming system" board would be necessary, based upon the disclosure of Weiss.

Appellants argue that "Weiss does not provide motivation for the modifications" (App. Br. 12). In my opinion, this situation represents a situation where "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR*, 550 U.S. at 416. "If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability." *Id.* at 417.

On reflection, I conclude that Appellants' argument relating to encryption is a diversion from the obviousness issue. Appellants claim is open, using "comprising" language and is permissive of encryption. The

transitional term "comprising" is "inclusive or open-ended and does not exclude additional, unrecited elements or method steps." *Georgia-Pacific Corp. v. U. S. Gypsum Co*., 195 F.3d 1322, 1327 (Fed. Cir. 1999). Therefore, Appellants' use of the term "comprising" permits the presence of additional elements, such as the encrypted communication between boards of Weiss. Like our appellate reviewing court, I "will not read into a reference a teaching away from a process where no such language exists." *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co*., 464 F.3d 1356, 1364 (Fed. Cir. 2006).

In my opinion, given that the function of a PCI, ISA, VME, or AGP protocol is to transmit data between two different computer boards, there is no reason to interpret these protocols as preventing the data from being encrypted while being transferred. In Weiss, it is not the RS-232 cable which encrypts and decrypts the information, but rather it is the processors in the "black" and "white" boxes. Consequently, when the ordinary artisan substitutes a PCI, ISA, VME, or AGP for the RS-232 cable, it will still be the processors in the "black" and "white" boxes which encrypt and decrypt the information. The PCI, ISA, VME, or AGP simply represent an alternate way in which the data is transferred between the processors in the "black" and "white" boxes. The transfer device, whether RS-232 cable or PCI bus is not concerned with whether the binary data being transmitted is encrypted or unencrypted.

I would affirm the rejections under 35 U.S.C. § 103(a) of claims 10, 11, 15, 16 and 20-24 as obvious over the combination of Weiss and Byers.

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